EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Exam 1

Fall 2020

Instructions: There are 10 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam, on separate sheets of white paper, or on a tablet pc. When finished, scan or image and upload as a .pdf file on Canvas. Exams are due by 1:00 p.m.

If parameters of semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/V^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=8fF/\mu^2$, $\lambda = 0$. If reference to a diode is made, assume the process parameter $J_S=10^{-17}A/\mu^2$. The ratio of Boltzmann's constant to the charge of an electron is k/q= 8.61E-5 V/K. If any other process parameters for MOS devices are needed, use the process parameters associated with the process described on the attachment to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters

Short Answer Questions

1. (2pts) Give one element that is used for doping silicon to form an n-type region?

2. (2pts) If the average annual sales per employee in the semiconductor industry is $500,000, approximately how many employees are there worldwide in the semiconductor industry?

3. (2pts) If a microprocessor is operating with a 1.5V supply and is dissipating 100W, what is the current drawn from the 1.5V power supply?

4. (2pts) Though high yields are common in the semiconductor industry, it would be highly unlikely to expect a 99.9999% yield. What is the major reason that such a high yield should not be required?

5. (2pts) When laying out transistors, a "dogbone" contact is often used to make contact to the gate. Why is the dogbone contact used?

6. (2 pts) What is one of the major advantages of Pass Transistor Logic?

7. (2pts) What is one of the major limitations of pass transistor logic?

8. (2pts) Why are all contacts typically of the same size in a CMOS process?

9. (2pts) If the gate dielectric for an n-channel transistor is made of SiO_2 and it is 50 Angstroms thick, about how many layers of SiO_2 molecules will be stacked on top of each other to form this gate dielectric?

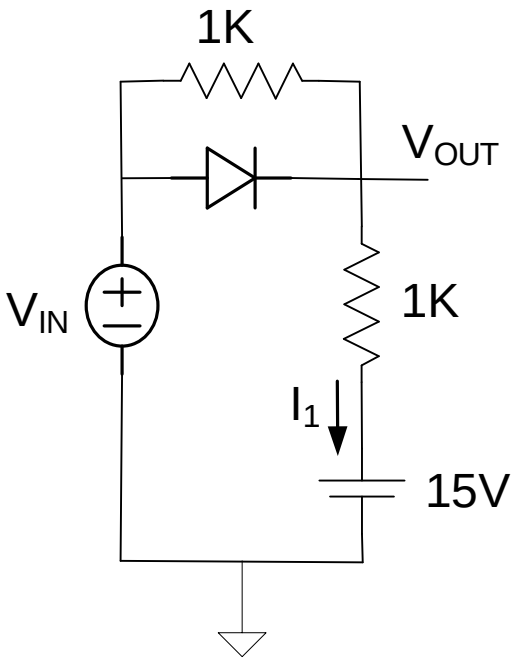
10. (2pts) The term MOS Transistor has been used for several decades to describe the transistors we have to work with in a standard CMOS process. But the acronym "MOS" is no longer descriptive of the structure of these transistors. What part of this acronym is no longer descriptive of these devices?

Problem 1(16 pts) If a die has an area of 1.5cm^2 in a process where 8" wafers cost $1500, determine the cost per good die if the defect density is 1.5/cm^2.

Problem 2 (16 pts)) Consider the following circuit. Assume the area of the diode is $100\mu m^2$.

a) Determine the current I_1 if $V_{IN}=5V$

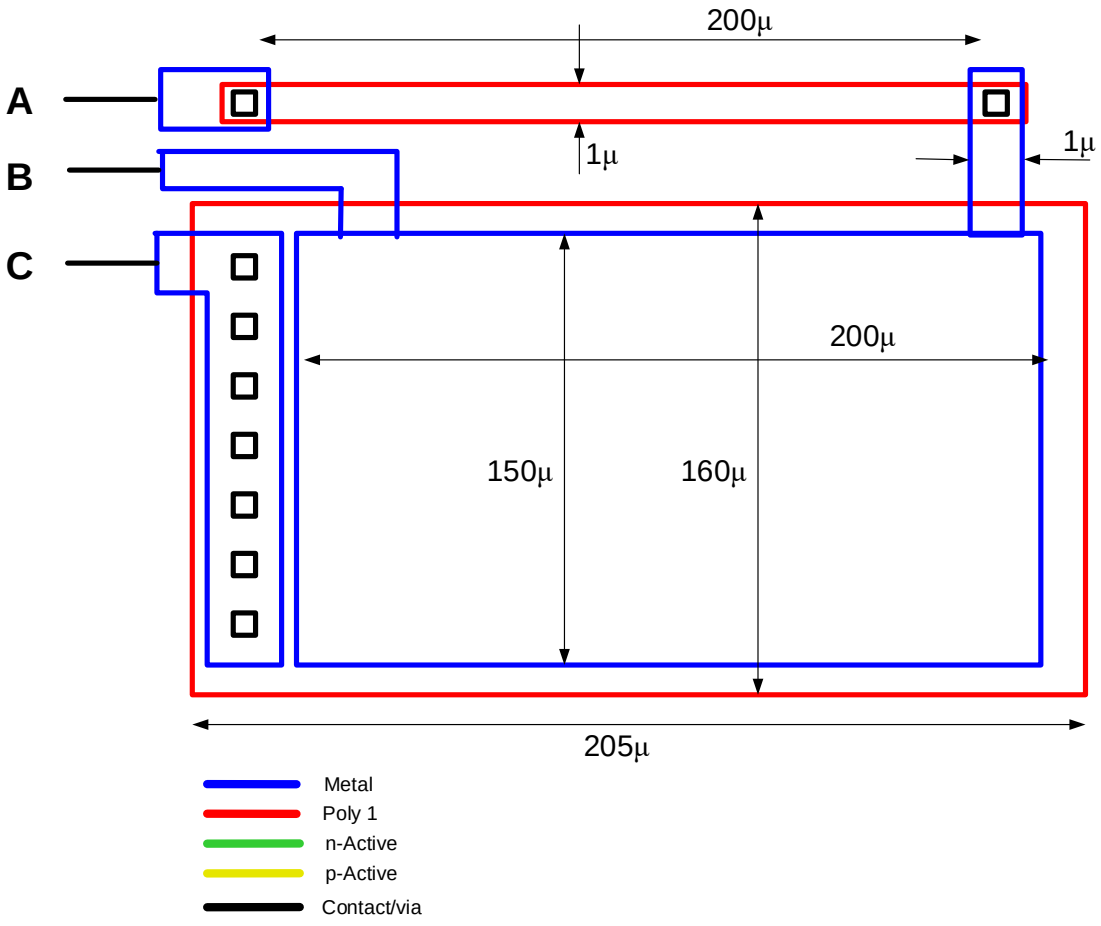
b) Obtain an expression for and plot V_{OUT} (t) for $0 < t < 2$ sec if $V_{IN}(t)= -40+40t$



Problem 3 (16 pts) The layout of a simple circuit is shown. For the purpose of being able to show sufficient detail on this exam, the layout is not to scale but the critical dimensions are indicated.

a) Give a schematic of this circuit (neglect the capacitances associated with 200µm x 1µm polysilicon rectangle connected to node A and neglect any capacitances associated with the substrate).

b) If node C is grounded, determine t_{LH} on node B if a step input is applied to node A. Accuracy of ±30% is good enough.



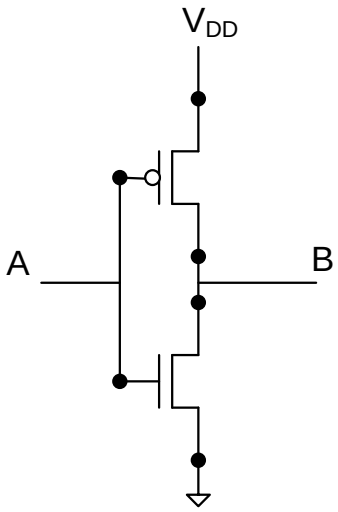
Problem 4 (16 pts) Consider a 5K resistor that is made by the parallel combination of two resistors. One of the resistors, designated as R_1, is made from n doped polysilicon with a TCR of -600 ppm/^oC and a sheet resistance of 100 Ω/□ and the other, designated as R_2, is made of a p-doped silicon with a TCR of 1000 ppm/^oC and a sheet resistance of 40Ω/□. Assume both are of the same physical dimensions with an effective length of L and width of W= 1μm.

a) Determine L for the resistors
b) Determine R_1 and R_2
c) Determine the TCR of the parallel combination

Problem 5 (16 pts)

Consider the CMOS Inverter shown below with minimum-sized transistors designed in the ON 0.5µm CMOS process where V_{DD}=3V. When the switch-level model is used with the series resistors in the drain, it is usually assumed that either the n-channel or the p-channel switch is closed and the other is open. Assume that for some intermediate input voltage at the A input, both switches are closed but the resistance remains at the same value that is used in the existing model. (In a real CMOS inverter, when the input transitions between the high and low state, there is a region where both transistors are conducting thereby causing the inverter to dissipate power. We generally try to change states quickly to limit the energy consumed during the transition.)

a) Determine the output voltage if both switches are closed
b) If a circuit has 10 million minimum-sized inverters, what would the power dissipation be if all of were stuck in the state where both switches are closed?



MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5µm
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	**83.5**	**105.3**	**23.5**	**999**	**44.2**	**0.09**	**0.10**	ohms/sq
Contact Resistance	**64.9**	**149.7**	**17.3**		**29.2**		**0.97**	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	**0.05**	**824**	**816**	ohms/sq
Contact Resistance	**0.79**			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	**425**	**731**	**84**		**27**	**12**	**7**	**37**	aF/um^2
Area (N+active)			**2434**		**35**	**16**	**11**		aF/um^2
Area (P+active)			**2335**						aF/um^2
Area (poly)				**938**	**56**	**15**	**9**		aF/um^2
Area (poly2)					**49**				aF/um^2
Area (metal1)						**31**	**13**		aF/um^2
Area (metal2)							**35**		aF/um^2
Fringe (substrate)	**344**	**238**			**49**	**33**	**23**		aF/um
Fringe (poly)					**59**	**38**	**28**		aF/um
Fringe (metal1)						**51**	**34**		aF/um
Fringe (metal2)							**52**		aF/um
Overlap (N+active)			**232**						aF/um
Overlap (P+active)			**312**						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		95.31	MHz
D256_WIDE (31-stg,5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.01	uW/MHz/gate